// VerilogA for ADC\_Class, IdealDAC\_10bit, veriloga

`include "constants.vams"

`include "disciplines.vams"

module IdealDAC\_10bit(d0,d1,d2,d3,d4,d5,d6,d7,d8,d9,vout,vdd,vss,vmin,vmax);

parameter real vtrans=0.5;

parameter real delay = 0;

parameter real ttime = 1p;

inout vdd,vss;

input d0,d1,d2,d3,d4,d5,d6,d7,d8,d9;

input vmin, vmax;

output vout;

electrical vout,vdd,vss,d0,d1,d2,d3,d4,d5,d6,d7,d8,d9,vmin,vmax;

real result,d\_0,d\_1,d\_2,d\_3,d\_4,d\_5,d\_6,d\_7,d\_8,d\_9;

analog begin

d\_9 = V(d9)\*512;

d\_8 = V(d8)\*256;

d\_7 = V(d7)\*128;

d\_6 = V(d6)\*64;

d\_5 = V(d5)\*32;

d\_4 = V(d4)\*16;

d\_3 = V(d3)\*8;

d\_2 = V(d2)\*4;

d\_1 = V(d1)\*2;

d\_0 = V(d0)\*1;

result = ((d\_9+d\_8+d\_7+d\_6+d\_5+d\_4+d\_3+d\_2+d\_1+d\_0) \* ((V(vmax)-V(vmin))/(1023))) + V(vmin) ;

V(vout) <+ transition(result,delay,ttime);

end

endmodule